

TOWARDS MODULE EFFICIENCIES OF 16% WITH AN IMPROVED CIGSSE DEVICE DESIGN

Thomas Dalibor, Stefan Jost, Helmut Vogt, Andreas Heiß, Sven Visbeck, Thomas Happ, Jörg Palm, Alejandro Avellán, Thomas Niesen and Franz Karg

AVANCIS GmbH & Co. KG, Otto-Hahn-Ring 6, 81739 Munich, Germany
Phone: +49-89-219620-550, Fax: +49-89-219620-502, e-mail: thomas.dalibor@avancis.de

ABSTRACT: Cu(In,Ga)(S,Se)₂ (CIGSSe) thin film modules based on the AVANCIS SEL-RTP process (stacked elemental layer – rapid thermal processing) are commercially available under the brand name PowerMax® in six different nominal power classes up to 135W, corresponding to a maximum aperture efficiency of 14.2%. In order to further catch up with multicrystalline silicon based solar modules we investigate advanced CIGSSe process and device designs in the AVANCIS R&D pilot line on 30*30cm²-sized substrates. With the improved CIGSSe device design which is the subject matter of the present publication we were able to further enhance the aperture area efficiency to an independently confirmed value of 15.5%. We report on the individual measures of the improved CIGSSe device design which resulted in an enhancement mainly of the fill factor FF. The efficiency improvement is achieved without compromising on the long-term stability of the electrical performance parameters as demonstrated by the results of a damp heat testing of several prototypes with the improved CIGSSe device design yielding comparable long-term stability data to our standard baseline products.

Along the routes described above the efficiency evolution further continues with the latest champion module coming from our line showing an independently certified aperture area efficiency of 15.8%.

Keywords: CIGS, High-Efficiency, Stability

1 INTRODUCTION

CIS solar cells show the highest efficiencies among all thin film technologies. Even though lab cell champion efficiencies of CIS devices on small areas have been demonstrated on par with multicrystalline silicon based solar cells, larger area, product-sized modules based on CIS need to catch up with high end multicrystalline modules. It is our clear intention at AVANCIS to close this efficiency gap in the near future. The achievement of a first intermediate milestone in our R&D program was reported at the last PVSEC in 2010 [1] with an independently confirmed aperture area efficiency of 15.1% for a 30*30cm² CIGSSe module. In this paper we report on a further important milestone towards our goal of driving efficiencies above 16%.

The Cu(In,Ga)(S,Se)₂ (CIGSSe) thin film modules based on the AVANCIS SEL-RTP process (stacked elemental layer – rapid thermal processing) are commercially available under the brand name PowerMax® in six different nominal power classes up to 135W, corresponding to aperture area efficiencies of up to 14.2%.

In the present publication we report on an improved CIGSSe device design demonstrated on 30*30cm²-sized substrates. The devices have been processed in the AVANCIS R&D pilot line and reach an aperture area efficiency of 15.5%. The improved device design is partly based on new process developments which will find their way into new industrial mass-production processes in due course.

In addition, we will present first data on our latest champion module with an independently certified aperture area efficiency of 15.8%.

2 BASELINE PROCESS SEQUENCE

The stacked elemental layer – rapid thermal processing (SEL-RTP) is the core part of the AVANCIS baseline manufacturing sequence and has previously been

reported in detail [1], [2], [3]. The manufacturing sequence is sketched in Fig. 1. It starts with the soda-lime glass covered by a silicon nitride (SiN) alkali-barrier layer and the molybdenum (Mo) back electrode as a substrate. After the P1 laser patterning, the first step in the CIGSSe absorber formation is the elemental precursor film deposition consisting of DC-magnetron sputtering of Cu-In-Ga:Na and thermal evaporation of selenium (Se). The second step is the reaction of the elemental precursor stack to form the CIGSSe semiconductor. Rapid thermal processing (RTP) is conducted in an infrared heated furnace capable of high heating rates in a sulfur containing ambient. The CdS buffer layer is deposited in a chemical bath deposition process, the ZnO:Al window layer by magnetron sputtering. In the baseline process mechanical scribing is applied for the patterning of the absorber (P2) and the ZnO (P3). Before lamination, the thin film is edge deleted and a bus bar is contacted to the Mo back electrode by ultrasonic welding. The standard module size is 30*30cm² for the R&D pilot line. An anti-reflective (AR) coated front glass is used to increase the short-current density as described in [1].



Figure 1: AVANCIS baseline process sequence.

3 EXPERIMENTAL

As a further important intermediate milestone in our R&D program we report on an improved CIGSSe device design demonstrating a module aperture area efficiency of 15.5%. The following individual measures were taken to enhance mainly the fill factor FF with respect to the previous champion device of the first milestone:

- a substitution of the P2 mechanical scribing by picosecond (ps) laser P2 scribing enabling a further reduction of the dead area width imposed by the spacing between P1 and P3 patterning lines for serial connection of the individual cells;
- an optimization of the cell design with a reduction of the cell width exploiting the reduced dead area width;
- an optimization of the window layer properties for the improved cell design with lowered sheet resistance and increased light transmittance.

The dead area width per cell was reduced by another 30% with respect to the previous champion device. The cell width was reduced by approx. 20% in comparison to the previous champion. Window layer deposition processing was adjusted in a way to improve the Haacke factor (Haacke factor = $\text{Transmission}^{10} / R_{\square}$) by approx. 80% with respect to the factor for the previous champion device.

4 RESULTS AND DISCUSSION

4.1 P2 laser patterning

State-of-the-art mechanical P2 scribing was substituted with a P2 laser scribing using a ps laser process.

Since the mechanical scribing process always causes chipping around the patterning lines, the reduction of the dead area width is limited especially for the P2 scribe in two ways: (1) when the width between P1 and P2 is smaller than the chipping width, ablated CIGSSe extends beyond the P1 scribe, thus causing ohmic shunts between the Mo back contact and the later on deposited window layer; (2) the mechanical P3 scribing process does not work properly on areas being affected by the P2 chipping, because of the direct contact of ZnO and Mo.

Fig. 1 shows an example of a ps laser P2 scribe imaged with (a) an optical microscope and (b) a confocal microscope.

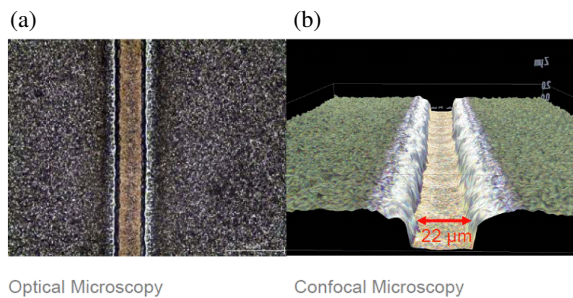


Figure 1: Optical microscope (a) and confocal microscope (b) picture of a ps laser P2 scribe sample. The P2 scribe width in this example is 22 μm .

Fig. 1a proves that the CIGSSe absorber is completely removed in the P2 scribe (brown line). Only minor residues on top of the Mo layer are left appearing yellowish in the confocal microscopy image of Fig. 1b. Both optical and confocal microscope images depict that the trench edge of the P2 scribe is clearly cut without any chipping.

A more detailed study of the newly developed laser patterning process is reported in another contribution to this 26th EU PVSEC conference [4]. This study could in

addition demonstrate that ps laser P2 processing reduces the contact resistance of the P2 interconnection of the modules, thus helping to lower the series resistance and increasing the fill factor.

4.2 Reduction of dead area width

The reduction of the dead area width between the P1 to P3 patterning lines by 30% with respect to the previous champion device is achieved without an increase in shunting.

Fig. 2 depicts thermographic images of the complete 30*30cm² circuits (a) for the previous champion device and (b) for the improved CIGSSe device design. The images are recorded in lock-in technique under pulsed forward bias with an infrared camera system. Bright spots in the image correspond to a local temperature increase as a result of shunting, e.g. due to insufficient spacing between the patterning lines, thus providing a shunt path in the serial connection of the individual cells. As can be seen in Fig. 2 there is no major difference in the number of bright spots between the previous champion design and the improved CIGSSe device design proving that the reduction of dead area width is achieved without additional shunting.

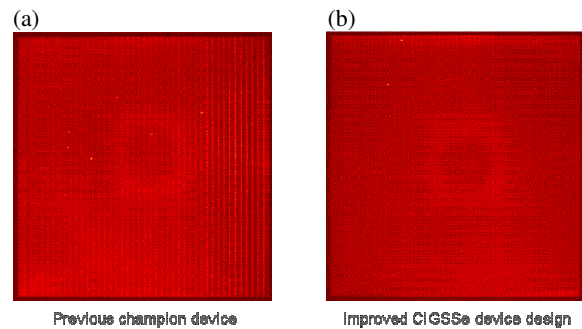


Figure 2: Thermographic images of the complete 30*30cm² circuits (a) for the previous champion device and (b) for the improved CIGSSe device design recorded under pulsed forward bias with an infrared camera system.

The reduction of the dead area width by the ps laser P2 processing is mainly exploited for the reduction of the cell width optimizing the cell design. The ratio a/L between dead area width a and active area width L is only slightly reduced by ~6%. The reduced cell width leads to a shorter transition path length of charge carriers in the window layer, thus lowering the series resistance of the module and raising FF.

4.3 Optimization of the window layer

The ZnO:Al window layer sputtering process was optimized in a way to improve the Haacke factor by approx. 80% with respect to the previous champion device. This enhancement of the Haacke factor was achieved both by a lowered sheet resistance of the window layer as well as by an increased light transmittance through the window layer as depicted in Fig. 3.

The better electrical conductivity of the window layer additionally lowers the series resistance and raises the fill factor.

The increased light transmittance also helped to slightly improve the short-circuit current J_{sc} .

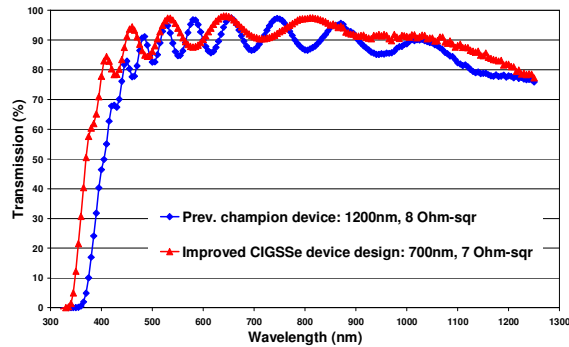


Figure 3: Transmission as a function of wavelength for ZnO:Al window layer on glass substrate as used (a) in the previous champion device and (b) in the improved CIGSSe device design.

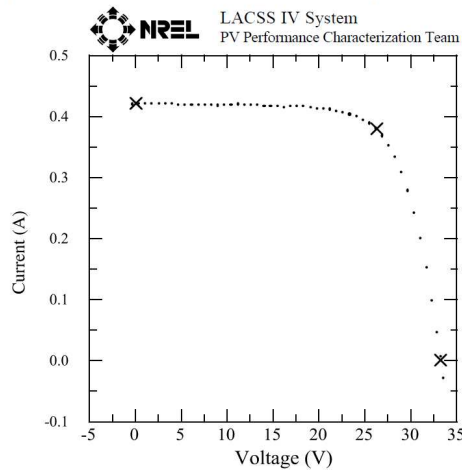
4.4 Certified I-V characteristics of the improved CIGSSe device design

Fig. 4 shows the results of an I-V measurement of one prototype of our improved CIGSSe device design. This measurement was conducted by the National Renewable Energy Laboratory (NREL, Col. USA) and certified an aperture area efficiency of 15.5% for an aperture area of 642.6cm² with $V_{oc}/cell=594mV$, $J_{sc}= 36.7mA/cm^2$ and FF=71.0%.

The NREL certification measurement agrees very well with our in-house measurement results at STC with a constant light solar simulator yielding $\eta_{aperture}=15.6%$, $V_{oc}/cell=590mV$, $J_{sc}=36.5mA/cm^2$ and FF=72.3%.

Avancis GmbH & Co. KG Germany
CdS/Cu(In,Ga)(S,Se) module

Device ID: 3881-5030C-EM Device Temperature = 24.3°C
 Nov 12, 2010 11:35:45 MT Device Area = 642.6 cm²
 Spectrum: ASTM G173 global Irradiance = 1000.0 W/m²



$V_{oc} = 33.25 V$ $V_{max} = 26.23 V$
 $I_{sc} = 0.4206 A$ $I_{max} = 0.3786 A$
 Fill Factor = 71.0% $P_{max} = 9.931 W$
 Efficiency = 15.5%

Device Dimensions = 25.4 x 25.3 cm
 Light soaked outdoors Global 0.222kWhr/m², Taped aperture

Figure 4: Certified I-V characteristics of a 30*30cm² module with improved CIGSSe device design.

Fig. 5 displays the shares of the three solar cell parameters V_{oc} , J_{sc} and FF in the overall efficiency enhancement of the new device design as compared to the previous champion device. The relative V_{oc} loss of -0.8% is balanced by a nearly equal relative J_{sc} gain of +0.9% resulting from the reduced dead area width and the improved window layer light transmittance. The efficiency enhancement of almost 4 % relative for the new device design is dominated by the relative FF gain of approx. +3.7%. The FF gain is mainly caused by the reduction of the series resistance. The new ps laser processing for the P2 scribe enabled the reduction of the dead area width, thus allowing the new device design with reduced cell width and a therefore optimized window layer with an increased electrical conductivity. The ps laser P2 processing in addition helped to reduce the contact resistance of the P2 interconnection, thus lowering the series resistance as well.

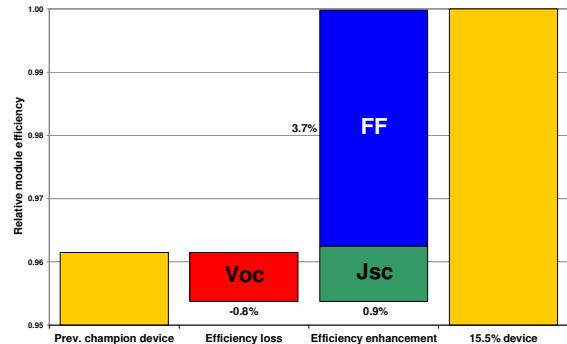


Figure 5: Contributions of the three solar parameters V_{oc} (red bar), J_{sc} (green bar) and FF (blue bar) to the efficiency enhancement of the improved CIGSSe device design as compared to the previous champion device [1].

4.5 Long-term stability of the improved CIGSSe device design

The validation of the new device design with respect to the long-term stability of the electrical performance parameters was done by subjecting several prototypes with the improved CIGSSe device design to climate testing. Fig. 6 depicts the results of a damp heat testing of these prototypes in relation to the baseline performance.

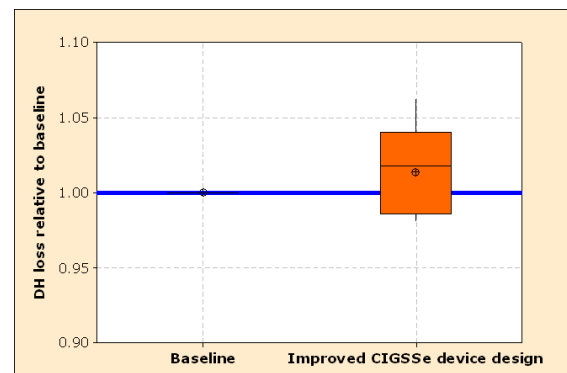


Figure 6: Relative long-term stability of the improved CIGSSe device design subjected to damp heat testing as compared to baseline device.

The improved CIGSSe device design shows a long-term stability of the electrical parameters comparable to the previous baseline products. Thus, the efficiency enhancement of the new device design is achieved without compromising the long-term stability of the electrical performance parameters.

4.6 Evolution of efficiency improvements

Fig. 7 provides an overview of the evolution of efficiency improvements of the last years for the R&D pilot line (30x30cm² Pilot Champion and 30x30cm² Pilot Average) as well as for the first manufacturing line of 20MW/a (65x160cm² Fab1 Average). Since the first manufacturing line went online in 2009 a steady improvement in module efficiency has been achieved. Of course, this is in part due to a steady maturing and tuning of the manufacturing line during the production ramp-up. Yet, the fast efficiency ramp-up was also partly enabled by leveraging the know-how stemming from 30 x 30 cm² Champion and Average efficiency evolution in the R&D pilot line.

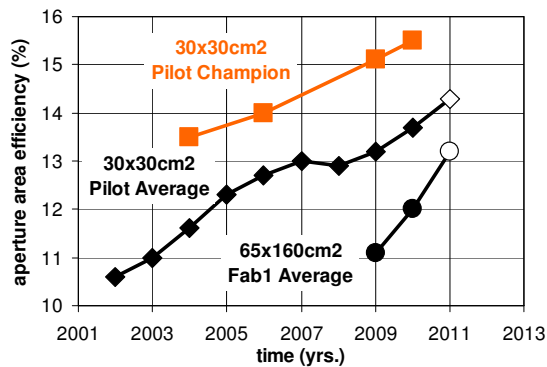


Figure 7: Evolution of the aperture area efficiency for the R&D pilot line (30x30cm² Pilot Champion and 30x30cm² Pilot Average) as well as for the first manufacturing line of 20MW/a (65x160cm² Fab1 Average). Open symbols mark the plan values.

Despite the achieved steady increase of the aperture area efficiency over the last years there is no saturation yet on the horizon limiting further efficiency improvements both for the 30*30cm² R&D modules as well as for the PowerMax® production modules. There is some headroom left as the most efficient of the so-called 2nd generation or thin-film PV products have not even reached half of the theoretically possible efficiency of 33% [5]. Also with respect to today's laboratory champion cells of 20.3% [6] the 30x30 champion with 15.5% reaches so far three-fourths of the efficiency.

4.7 Certified I-V characteristics of the latest champion module

Fig. 8 shows the results of an I-V measurement of our latest champion module. This measurement was conducted by the TÜV Rheinland (Cologne, Germany) and certified an aperture area efficiency of 15.8% for an aperture area of 640.05cm².

An aperture area efficiency of 15.8% is according to the most recent "Solar cell efficiency tables – Version 38" in [7] the highest independently confirmed efficiency for a thin-film module.

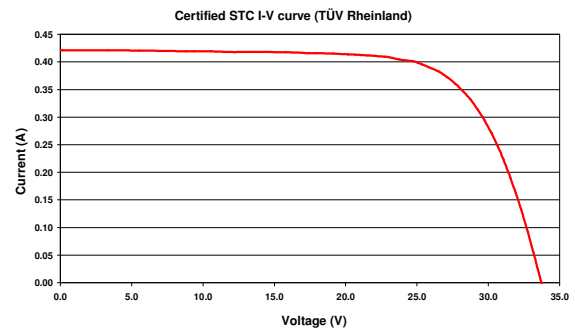


Figure 8: Certified I-V characteristics of our latest champion module.

For our latest champion module we reduced the CIGSSe absorber thickness by approx. 10% and optimized the SEL-RTP process for the thinner absorber. In addition, we continued to improve the ps P1 laser processing and further reduced the P1 – P3 dead area.

5 CONCLUSION

We have demonstrated an independently certified module aperture area efficiency of 15.8% for our latest Champion module with reduced CIGSSe absorber thickness and optimized SEL-RTP process in combination with ps P1 laser processing and further reduced P1 – P3 dead area.

According to the most recent "Solar cell efficiency tables – Version 38" in [7] this is the highest efficiency independently confirmed for a thin-film module.

For a CIGSSe device design with an independently certified module aperture area efficiency of 15.5% we described in detail the improvement of the fill factor with a relative gain of 3.7% related to the previous champion device with 15.1% efficiency.

The FF-improved CIGSSe device design comprises the substitution of P2 mechanical scribing by ps laser P2 scribing, the reduction of P1 – P3 dead area width between the patterning lines, the optimization of the cell design exploiting the reduced dead area and the optimization of the ZnO:Al window layer properties with lowered sheet resistance and increased light transmittance.

The results of the damp heat testing of several prototypes with improved CIGSSe device design proved that the new design achieves long-term stability of the electrical performance parameters comparable to the previous baseline products.

Leveraging the know-how of this new champion module with 15.8% efficiency will help to further evolve the efficiency of the AVANCIS PowerMax® modules both for the operational 20MW/a manufacturing line as well as for the upcoming two 100MW/a manufacturing lines. Further steps towards increased prototype module efficiency are in the pipeline to continue the evolution of efficiency improvements.

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